**Claims:**

1. A quadrature modulator, comprising:

a) an in-phase modulation branch receiving as an input an analog in-phase base band signal, the in-phase modulation branch including a first dc offset adjustment circuit, a first base band gain adjustment circuit, and a first mixer;

b) a quadrature modulation branch receiving as an input an analog quadrature based band signal, the quadrature modulation branch including a second dc offset adjustment circuit, a second base band gain adjustment circuit, and a second mixer;

c) a local oscillator means for providing a local oscillator signal to the first mixer and a phase shifted version of the local oscillator signal to the second mixer;

d) a summer for summing the outputs of the first and second mixers;

e) an envelope detector for detecting an output signal of the modulator and providing a signal representative of the amplitude of the output signal;

f) a band pass filter for filtering the amplitude signal; and

g) a signal strength indicator circuit for measuring the strength of the filtered amplitude signal, the indicator circuit providing a compensation signal for adjusting the phase shift of the local oscillator and the dc offsets and base band gains of the in-phase and quadrature base band signals.

2. A modulator according to claim 1, wherein the envelope detector is a synchronous detector and the signal strength indicator is a log indicator.

3. A modulator according to claim 2, including a programmable attenuator for adjusting the level of the output signal, and wherein the envelope detector measures the output signal following attenuation.

4. A modulator according to claim 1, including a tone generator for supplying a test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the test tone signal to the quadrature modulation branch input.

5. A modulator according to claim 4, including means for:

a) applying a first test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the first test tone signal to the quadrature modulation branch input;

b) employing the compensation signal to minimize carrier leakage in the output signal by adjusting the base band dc offsets in the in-phase and quadrature branches;

c) applying a second test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the second test tone signal to the quadrature modulation branch input, wherein the second test tone has a frequency that is substantially one half of the frequency of the first test tone; and

d) employing the compensation signal to minimize an undesired upper sideband frequency component in the output signal by adjusting the base band gains the in-phase and quadrature modulation branches and the phase shift of the local oscillator signal.

6. A method of calibrating a quadrature modulator, comprising:

a) applying a first test tone signal to an in-phase modulation branch input of the modulator and a ninety degree phase-shifted version of the first test tone signal to a quadrature modulation branch input of the modulator;

b) measuring the level of a local oscillator (LO) feedthrough in an output signal of the modulator and in response adjusting base band dc offset voltages to minimize the LO feedthrough;

c) applying a second test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the second test tone signal to the quadrature modulation branch input; and

d) measuring the level of an undesired upper sideband frequency component in the output signal and in response adjusting base band gains the in-phase and quadrature modulation branches and a LO phase error to minimize the undesired sideband.

7. A method according to claim 6, wherein the second test tone has a frequency that is substantially one half of the frequency of the first test tone.

8. A method according to claim 6, wherein measuring the level of the local oscillator (LO) feedthrough or the USB in the output signal is carried out by:

a) shifting the frequency spectrum of the output signal such that a lower sideband frequency component (LSB) is down-converted to zero IF;

b) filtering the spectrum-shifted signal to pass through either the LO feedthrough or the USB; and

c) measuring the amplitude of the filtered, spectrum-shifted signal.

9. A method according to claim 8, wherein the frequency spectrum of the output signal is shifted by a synchronous envelope detector.

10. A method according to claim 9, wherein the synchronous envelope detector comprises:

a) a Gilbert cell having at least one differential transistor pair in an upper branch and at least one transistor in a lower branch, the upper and lower branches being interconnected , each of the upper and lower branches having input terminals;

b) a resistor divider network connected between the input terminals of the upper branch and the input terminals of the lower branch, the resistive values of the network being selected such that a selected input signal having a signal level sufficient to saturate the transistors of the upper branch is attenuated so as to not saturate the transistors of the lower branch; and

c) low pass filter means connected to the upper branch of transistors, an output signal of the detector being provided at the low pass filter.

11. A method according to claim 8, wherein the amplitude of the filtered, spectrum-shifted signal is measured by a log detector which provides a compensation signal employed to minimize the LO feedthrough or undesired sideband.

12. A method according to claim 11, including selectively attenuating the output signal prior to the step of measuring the output signal.

13. A method according to claim 11, wherein the second test tone has a frequency that is substantially one half of the frequency of the first test tone.

14. A quadrature modulator, comprising:

a) an in-phase modulation branch receiving as an input an analog in-phase base band signal, the in-phase modulation branch including a first dc offset adjustment circuit, a first base band gain adjustment circuit, and a first mixer;

b) a quadrature modulation branch receiving as an input an analog quadrature based band signal, the quadrature modulation branch including a second dc offset adjustment circuit, a second base band gain adjustment circuit, and a second mixer;

c) a local oscillator means for providing a local oscillator signal to the first mixer and a phase shifted version of the local oscillator signal to the second mixer;

d) a summer for summing the outputs of the first and second mixers;

e) envelope detection means for detecting an output signal of the modulator and providing a signal representative of the amplitude of the output signal;

f) band pass filter means for filtering the amplitude signal; and

g) a log detector for measuring the strength of the filtered amplitude signal, the log detector providing a compensation signal for adjusting the phase shift of the local oscillator and the dc offsets and base band gains of the in-phase and quadrature base band signals.

15. A modulator according to claim 14, including calibration means for:

a) applying a first test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the first test tone signal to the quadrature modulation branch input;

b) employing the compensation signal to minimize carrier leakage in the output signal by adjusting the base band dc offsets in the in-phase and quadrature branches;

c) applying a second test tone signal to the in-phase modulation branch input and a ninety degree phase-shifted version of the second test tone signal to the quadrature modulation branch input, wherein the second test tone has a frequency that is substantially one half of the frequency of the first test tone; and

d) employing the compensation signal to minimize an undesired upper sideband frequency component in the output signal by adjusting the base band gains the in-phase and quadrature modulation branches and the phase shift of the local oscillator signal.

16. A synchronous envelope detector, comprising:

a) a Gilbert cell having at least one differential transistor pair in an upper branch and at least one transistor in a lower branch, the upper and lower branches being interconnected , each of the upper and lower branches having input terminals;

b) a resistor divider network connected between the input terminals of the upper branch and the input terminals of the lower branch, the resistive values of the network being selected such that a selected input signal having a signal level sufficient to saturate the transistors of the upper branch is attenuated so as to not saturate the transistors of the lower branch; and

c) low pass filter means connected to the upper branch of transistors, an output signal of the detector being provided at the low pass filter.

17. A detector according to claim 16, wherein the lower branch has two BJT transistors and a resistor is connected between the emitters of the transistors.

18. A detector according to claim 16, including means for biasing the transistors of the upper branch.